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ART UNIT	PAPER NUMBER
2187	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/731,788	SUKEGAWA, HIROSHI	
	Examiner	Art Unit	
	Glenn Gossage	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-14 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-14 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 08 December 2000 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 and 6 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. A new title such as --NONVOLATILE SEMICONDUCTOR MEMORY INCLUDING PLURAL MEMORY CIRCUITS SELECTIVELY CONTROLLED BY A CHIP ENABLE TERMINAL OR AN INPUT COMMAND AND WHICH MAY SIMULTANEOUSLY PERFORM WRITE OPERATIONS-- is suggested (see claim 1, lines 1-3 and 6-7; claim 5, lines 1-2 and 5-6; and claim 9, lines 1-2 and 6-8, e.g.). The loss in brevity of title is more than offset by the gain in its informative value in indexing, classifying, searching, etc. See MPEP 606 and 606.01.

3. The abstract of the disclosure is objected to because the language "In a ... memory device, ... the memory chip" in lines 1-3 (page lines 2-4) is not clear. The proper antecedent for "the memory chip" in line 3 is also not clear [note the plural memory chips in lines 2-3 (page lines 3-4), e.g.]. In lines 3-5 (page lines 4-6), the wording "each of which includes ... and which share" is not clear. The language "carrying out a writing sequential control" in lines 4-5 (page lines 5-6) is also not clear. The following changes are suggested: In line 1 (page line 2), change "In a" to --A--, and in line 3 (page line 4), change ", the" to -- . The--. In lines 4-5 (page lines 5-6), change "a writing sequential control and which" to --sequential writing control and which

EEPROM circuits share--. In line 7 (page line 8), before "carried" insert --simultaneously-- (note claim 9, lines 6-7, e.g.).

Additionally, in line 3 (page line 4), and throughout the abstract, the first occurrence of all acronyms or abbreviations should be written out for clarity, whether or not they may be considered "well known." Accordingly, "EEPROM" should be changed to --electrically erasable programmable read only memory (EEPROM)-- for clarity.

Also, one or two sentences should be added describing additionally claimed and disclosed features. [For example, in line 8 (page line 9), after "parallel.", insert sentences such as --The activity and inactivity of each of the EEPROM circuits may also be controlled by a logical combination of a master chip enable signal and a chip enable signal of each of the individual EEPROM circuits. A pass or fail result of writing operations may be output or held and accumulated, with the nonvolatile semiconductor memory device having modes of operation in which it is determined whether data may be inputted to a data buffer by selectively referring to a pass/fail result.-- See claims 3-4 and 9-14, e.g.]

Appropriate correction is required. See MPEP § 608.01(b).

4. The drawings are objected to because in Figure 2, within "box" 21, "MEMOR" should be --MEMORY-- for clarity. Also, it appears --NONVOLATILE-- should be inserted before

"MEMOR(Y)" for clarity and consistency (see page 4, lines 29-30, e.g.). In "box" 24, "DADA" should be --DATA-- for clarity and consistency (note page 5, line 1, e.g.).

In Figure 4, it appears "P" (four occurrences) should be --R-- (see page 6, line 24, e.g.). Also, it appears a representative one of the "boxes" should be labeled for clarity (using a label such as --EEPROM-- within "box" 2-1, e.g.).

In Figure 5, as well as Figure 6, it is not clear whether the address/data/command bus 3 should be shown as being connected or input to the memory function circuit 4 (in this regard, note page 7, lines 10-20, e.g.). Also see page 8, lines 12-25 with respect to Figure 6. Also, it appears the R/B signals from circuits 2-1 to 2-4 should be relabeled --R/B1-- to --R/B4-- for consistency (see Figures 1 and 3, e.g.).

In Figure 8, "DADA2(4)" should be --DATA2(4)-- for clarity. Also, it appears "CASH PROGRAM COMMAND" changed to --CACHE PROGRAM (WRITE START) COMMAND-- or other similar language for clarity and consistency (see page 10, lines 7-8, e.g.).

Applicant is REQUIRED to submit a proposed drawing correction in response to this Office action. However, actual formal correction of the noted defect(s) (submission of corrected formal drawings, e.g.) can be deferred until the application is allowed by the examiner.

Also note MPEP 608.02(r) and (v).

5. It is noted here that this application appears to contain claims directed to different inventions or different species of the same invention (here, an electrically rewritable nonvolatile semiconductor memory device). More specifically, the application contains claims (see claims 1-4 and 5-8, e.g.) directed to an electrically rewritable nonvolatile semiconductor memory device including control circuits for sequentially controlling writing and, in various embodiments, a chip enable terminal or an inputted command for controlling the inactivity and inactivity of the memory circuits. Other claims (see claims 9-14, e.g.) are directed to an electrically rewritable nonvolatile semiconductor memory device including plural memory circuits, each having at least one stage of a data buffer, writing operations being simultaneously carried out via the data buffer, and in which pass/fail results are outputted or accumulated.

While these inventions or species appear to be distinct, a restriction requirement is NOT being made at this time since it does not appear there will be a substantial burden on the Office if restriction is not required. However, restriction may be required in the future depending on how the claims are amended. In this regard, see MPEP 811, and also note the comments below with respect to 35 U.S.C. 112, second paragraph.

6. The disclosure has not been checked by the Examiner to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the disclosure. The following objections are specifically noted:

In the specification:

On page 1, line 6, it appears "Hei11" should be changed to simply --11-- or --Hei 11-- for clarity. In line 12, it appears --such as an electrically erasable programmable read only memory-- should be inserted before "(EEPROM)" for clarity and consistency (with the acronym). In line 33, it appears "Application Nos. 6-95125 and 6-95126" should be changed to --Publication (Kokai) Nos. 07-302175 and 07-302176-- for clarity.

On page 2, line 8, and throughout the specification, the first occurrence of all acronyms or abbreviations should be written out for clarity, whether or not they may be considered "well known." Accordingly, "CPU" should be changed to --central processing unit (CPU) for clarity.

On page 3, line 16, it appears "a plurality chip are" should be --plural chips are-- or --a plurality of chips is-- for clarity. In line 36, it appears --the-- should be inserted before "EEPROMs" for clarity. See also page 4, line 12.

O page 4, lines 34-35, "via an I/O buffer 26" should be set off by commas for clarity. Also, "I/O" in line 34 should be --input/output (I/O)--.

On page 5, line 12, the language "outputted from the chip enable terminals CE" is not entirely clear here, particularly when read in conjunction with Figure 2 and page 6, lines 8-9. [Should "outputted from" in line 12 be changed to --input to--?] In lines 14-15, the proper antecedent for "These control signals" is not clear here. [Are the enable signals also input to control circuit 29 in Fig. 2?] In line 17, it appears "is" should be deleted for clarity. In lines 33-34, it is not entirely clear what is meant by "to input/output data every small capacity unit."

On page 6, lines 13-14, the language "it is possible to decrease the number of enable signal lines which extend from a chip set" is not entirely understood here (when read in conjunction with Figures 1 and 3).

On page 6, lines 36-37, the proper antecedent for "the storage capacity resistor of the EEPROM circuits 2" is not clear here. Moreover, on page 6, line 36 to page 7, line 1, it is not clear how the chip set "refers to the storage capacity resistor of the EEPROM circuits 2 of the memory chips 1a1 and 1a2 to determine "0" or "1" of the master chip enable terminal."

On page 7, line 4, the wording "and address assignment which are host's requests" is not clear in this context. In line 14, it appears "outside" should be deleted or changed to --to the outside-- for clarity. In line 18, it is not clear to what "memory function selecting circuit 3" is being referred here. [Should "a memory function selecting circuit 3" be changed to --the memory function register 4--? See line 22 and Fig 5, e.g.] In line 23, it appears "enable" should be --enabled--. In lines 32-33, "any one of memory chips, the generation" appears to read more clearly as --any one of a number of memory chips, the generations--. In lines 35-36, it is not entirely clear what is meant by "a little control continues to enter each of the EEPROM circuits."

On page 8, line 14, it appears "different" should be --difference--. In line 16, it appears "has" should be --have--. In line 18, it appears "a" should be deleted. In line 34, it appears "a" reads more clearly here as --one--.

On page 9, lines 1-2, it is not clear what is meant by "wherein it is not felt that a plurality of EEPROM circuit functions are provided inside." In line 6, "two" should be --to--. Moreover, it is not clear what is meant by "to return the memory chip" in this context ("return" the memory chip where?). In lines 8-9, it is not clear what is meant by "high recovery." In lines 21-22, the language "Each of the EEPROM circuits 2 does not include any control circuits" is unclear and confusing when read in conjunction with lines 17-19. That is, if "commands, addresses and data (are allowed) to be inputted to the I/O buffer of each of the EEPROM circuits" as stated in lines 17-19, it would appear the EEPROM circuits would contain some "control circuits." In line 28, it appears "continuously" should be changed to --continuous--. In line 29, "in" appears to read more clearly here as --with--.

On page 10, line 10, it appears "circuit" should be --circuits--. In line 16, it is not clear what is meant by "When batch data transfer to the internal data is complete" ("data transfer to the ... data" is unclear). In line 22, the wording "can process the case of Fail" is not clear. In lines 29-30, the wording "about the presence of Fail during accumulation" is not clear. Similarly, in line 30, "the whole Pass/Fail" is unclear in this context. In line 36, the language "is carried out every EEPROM" is not clear.

On page 10, line 37 to page 11, line 1, the language "it is possible to carry out a processing in the case of Fail every EEPROM circuit" is unclear and confusing.

On page 11, line 1, ", and in" appears to read more clearly here as -- . In--. In line 13, "inputted In" should be --inputted. In-- for clarity. In line 16, it appears --one-- should be

inserted after "enabling" for clarity. In line 30, it appears "modification" should be --modifications-- for clarity.

Again note that these are merely exemplary. The entire specification should be carefully and completely reviewed to ensure that all possible errors are located and corrected.

In the claims:

In claim 1, line 4, "in" appears to read more clearly here as --on--. See also claim 5, line 4.

In claim 2, line 1, it appears --electrically rewritable-- should be inserted before "nonvolatile" for consistency (see claim 1, lines 1-2, e.g.). See also claims 3 and 4, line 1, as well as claims 6-8 and 10-14, line 1 (noting claims 5 and 9, line 1).

In claim 3, line 2, it appears "wherein" should be changed to --further comprising-- for clarity. Note that "and" (first occurrence) in line 4 should then be changed to --wherein-- for clarity. In line 7, it appears "of each of the memory circuits" should be deleted (note the language "of each of said memory circuits" in lines 4-5, e.g.).

In claim 4, lines 3-4, it appears "where ... are applied" reads more clearly here as --with ... as inputs-- or --having ... as inputs--.

In claim 5, line 2, it appears "having" should be --comprising:-- for clarity and consistency (see claim 1, lines 1-2, e.g.).

In claim 6, line 4, it appears --common-- should be inserted before "chip" for clarity and consistency (note line 2, e.g.).

In claim 7, line 2, it appears --said-- should be inserted before "memory" for clarity. In lines 2-3, "made enable" appears to read more clearly here as simply --enabled--.

In claim 8, line 6, it appears --common-- should be inserted before "ready/busy" for clarity and consistency (note line 2, e.g.).

In claim 9, line 2, it appears "wherein" should be changed to --comprising:-- for clarity (the claim language is somewhat functional as it is not entirely clear what makes up or comprises the electrically rewritable nonvolatile semiconductor memory as claimed) and consistency (see claim 1, lines 1-2, e.g.). Note that "are" in line 3 should then be deleted. Also, it appears "and" in line 3 should be deleted, and "is provided with" in line 4 changed to --including--, for clarity. In lines 4-5, "stage of data buffer" is not entirely clear. [Should --a-- simply be inserted before "data buffer" in claim 9, line 5?]

In claim 10, line 2, it appears --said-- should be inserted before "writing" for clarity.

In claims 13 and 14, line 2, it appears "which" should be changed to --wherein said nonvolatile semiconductor memory device-- for clarity.

Appropriate correction is required.

7. Claims 1-4, 7 and 9-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, and therefore its dependent claims, the language "a (singular) chip enable terminal ... provided for each of the memory circuits" is confusing and unclear. Is a (one) chip enable terminal provided for all (each) of the memory circuits? Are there a plurality of chip enable terminals, with one (a) chip enable terminal "provided for each of the memory circuits?" The proper antecedent for "said chip enable terminal" in claim 2, lines 3-4 and claim 3, lines 6-7 is also not completely clear since there are plural memory circuits, each (apparently) having a chip enable terminal. It appears "a chip enable terminal" in claim 1, line 5 should be changed to --a plurality of chip enable terminals-- and "each of the memory circuits provided" in line 7 changed to --the memory circuits, respectively provided-- for clarity. Also, "said" in claim 2, line 3 and claim 3, line 6 should then be changed to --a respective-- for clarity and consistency.

In claim 3, lines 3-4, it is not entirely clear how the master chip enable terminal controls the activity and inactivity of "said plurality of memory circuits as a whole." It appears "plurality of memory circuits" in line 3 should be changed to --memory chip-- for clarity and consistency (see page 6, lines 2-4, e.g.).

In claim 4, line 4, the proper antecedent for "the each chip enable terminal" is not entirely clear. It appears "the each" in line 4 should be changed to --a respective-- for clarity and consistency (in conjunction with the changes suggested for claim 1, e.g.).

In claim 7, it is not readily apparent how "two memory circuits are alternatively made enable(d) by said command" (support for language in the specification?). Note that while, in one embodiment, the master chip enable terminal is used to "alternatively activate" or enable two memory chips, each having a plurality of memory circuits (see page 6, lines 27-29 and Figure 4, e.g.), it is clear how "two of memory circuits are alternatively made enable(d) by said command" (see Figure 5 and its corresponding description in the specification).

In claim 9, and therefore its dependent claims, it is not entirely clear how the plurality of memory circuits are "able to assign an address" (support for language in the specification? See page 6, lines 31-36, e.g. discussing the embodiment of Figure 4.). [Should ", which are able to assign an address" in claim 9, lines 2-3 simply be deleted and "said" in line 6 changed to --an--?] It is also not readily apparent to where the at least one stage "transmits" the data (see line 5, e.g.). [Should "transmitting" in line 5 simply be changed to --storing--?] In lines 7-8, the proper antecedent for "said data buffer" is not entirely clear since there are plural memory circuits, each having "at least one (stage of) data buffer," set forth in the claims (see lines 4-5). It is also not entirely clear how the writing operations are carried out simultaneously "via said data buffer" (singular). [Should "via said data buffer" simply be deleted in claim 9, lines 7-8?]

In claim 11, lines 2-3, it is not clear what is meant by the pass/fail result is "outputted every memory cell" (support for language in the specification?).

In claims 11 and 12, the proper antecedent for "said pass/fail result" is not adequately clear since there are plural writing operations, each with a pass/fail result, set forth in the claims (see claim 10, lines 2-3, e.g.).

Also in claim 12, it is not clear how a (singular) pass/fail result is "accumulated." It is also not clear how or where plural pass/fail results would be "accumulated," much less "to be" held (it would appear "accumulated" results would necessarily have to be "held" somewhere).

In claims 13 and 14, the proper antecedents for "said data buffer" and "said pass/fail result" are unclear analogous to claim 9, lines 7-8 and claims 11 and 12.

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 9-10, insofar as definite and clear, are rejected under 35 U.S.C. 102(b) as being anticipated by Lee et al.

With respect to claim 9, Lee et al discloses an electrically rewritable nonvolatile semiconductor memory device such as an electrically erasable programmable read only memory (EEPROM) including a plurality of "memory circuits," provided in a memory chip, as in the present invention [see the EEPROM "memory circuits" including subarray 400-0 and associated circuits 402, 454 and 404 and subarray 400-3 and associated circuits 408, 460 and 410 in Figure 3 and column 3, lines 15-17 and 55-58, e.g.]. Lee et al discloses that each of the memory circuits is provided with at least one stage of a "data buffer" [see data registers 404, 405, 409 and 410 in Figure 3 and column 4, lines 46-49, e.g.] for transmitting writing data corresponding to the address, and also teaches that writing operations in the plurality of memory circuits may be simultaneously carried out "via" or using the data buffer in each of the memory circuits [see column 1, lines 14-51 and column 4, line 50 to column 5, line 7, e.g.].

With respect to claim 10, Lee et al discloses that the "pass/fail" results of each of the writing operations may be ascertained by corresponding program/verify circuits (such as 454 and 460 in Figure 3) and outputted to each of the respective memory circuits.

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sukegawa et al (U.S.'001) and Lee et al, taken together.

With respect to claim 1, Sukegawa et al ('001) discloses an electrically rewritable nonvolatile semiconductor memory device, such as an electrically erasable programmable read only memory (EEPROM), including a plurality of "memory circuits," each of which has a control circuit for sequentially controlling writing so as to share a data bus, as in the present invention. See EEPROM memory circuits 11-1 to 11-3 and 11-16 in Figure 2, as well as column 40, lines 55-65, e.g. Sukegawa et al (U.S. '001) also discloses a chip enable terminal provided for each of the memory circuits, for controlling the activity and inactivity of each of the memory circuits [see the chip enable terminals CE and signals CS1 to CS3 and CS16 in Figure 2, as well as column 14, lines 33-51, e.g.]. However, Sukegawa et al does not teach that the plurality of memory circuits are "provided in a memory chip."

Lee et al similarly discloses an electrically rewritable semiconductor memory device such as an EEPROM including a plurality of "memory circuits" which share a data bus, and also teaches that writing operations in the plurality of memory circuits may be simultaneously carried out in each of the memory circuits [see column 1, lines 14-51 and column 4, line 50 to column 5, line 7, e.g.]. Lee et al also teaches that the plurality of memory circuits may be "provided in a memory chip" [see column 3, lines 15-17 and 55-58, e.g.] with each of the memory circuits including control or enable signals to allow individual control of the writing operations in each of the memory circuits provided on the memory chip and coupled to the shared data bus [see EEPROM

"memory circuits" including subarray 400-0 and associated circuits 402, 454 and 404 and subarray 400-3 and associated circuits 408, 460 and 410 in Figure 3 and column 4, line 50 to column 5, line 7, e.g.]. As those of ordinary skill in the art would readily appreciate, integrating a plurality of similar circuits on an integrated circuit (IC) or "chip" allows the overall size and cost of the circuit to be decreased, and also provides fewer interconnections, increasing reliability.

Accordingly, it would have been readily obvious to one of ordinary skill in the art at the time the claimed invention was made to provide the plurality of EEPROM memory circuits in Sukegawa et al (U.S. '001) "in a chip," with each of the memory circuits including individual control and enable signals, as taught by Lee et al, in order to allow a "time sharing" control of a data bus coupled to the plurality of memory circuits and allow writing operations to be carried out in parallel in each of the memory circuits. The reduction in access time and increase in operating speed obtained by performing the writing operations in parallel, coupled with the well known benefits of smaller overall size and cost, and improved reliability, obtained by integrating or providing a plurality of circuits such as memory circuits "in a chip," provides ample motivation and suggestion to provide the plurality of memory circuits in Sukegawa et al "in a chip."

Since applicant's claims "read on" a structure and method rendered obvious to one of ordinary skill in the art by the combined teachings of the references, the invention as set forth in the claims would have been obvious, within the meaning of 35 U.S.C. 103, in light of the prior art.

With respect to claim 2, Sukegawa et al (U.S. '001) discloses that each of the memory circuits is provided with a ready/busy signal terminal which corresponds to a respective chip enable terminal [see the RDY/BUSY terminals in EEPROMs 11-1 to 11-3 and 11-16 and signals R/B1 to R/B3 and R/B16 in Figure 3, as well as column 14, lines 47-51 and column 18, lines 15-24, e.g.]

With respect to claims 3 and 4, Lee et al also discloses providing a "master" enable signal or terminal for controlling the activity and inactivity of the plurality of memory circuits "as a whole," with the activity and inactivity of each of the memory circuits being controlled by a logical output of the "master" enable signal and a signal of the chip enable terminal of each of the memory circuits [see the AND logic in Figures 6, 8 and 9, e.g., which outputs signals to respectively control the "activity" and "inactivity" of circuitry within each of the memory circuits].

10. Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sukegawa et al (U.S.'001) and Lee et al, taken together.

With respect to claim 5, Sukegawa et al ('001) discloses an electrically rewritable nonvolatile semiconductor memory device, such as an electrically erasable programmable read only memory (EEPROM), including a plurality of "memory circuits," each of which has a control circuit for sequentially controlling writing so as to share a data bus, as in the present invention (see EEPROM memory circuits 11-1 to 11-3 and 11-16 in Figure 2, as well as column 40, lines 55-65,

e.g.). Sukegawa et al ('001) also generally discusses that the "activity" and "inactivity" of each of the memory circuits may be controlled "by inputting a command" (Sukegawa et al teaches that in response to certain commands, memories may be made "active" or "inactive" for write and read operations--see column 28, lines 29-49, e.g.), but does not teach that the plurality of memory circuits are "provided in a memory chip."

Lee et al similarly discloses an electrically rewritable semiconductor memory device such as an EEPROM including a plurality of "memory circuits" which share a data bus, where writing operations in the plurality of memory circuits may be simultaneously carried out in each of the memory circuits [see column 1, lines 14-51 and column 4, line 50 to column 5, line 7, e.g.]. Lee et al further teaches that the plurality of memory circuits may be "provided in a memory chip" [see column 3, lines 15-17 and 55-58, and also see EEPROM "memory circuits" including subarray 400-0 and associated circuits 402, 454 and 404 and subarray 400-3 and associated circuits 408, 460 and 410 in Figure 3 and column 4, line 50 to column 5, line 7, e.g.]. As those of ordinary skill in the art would readily appreciate, integrating a plurality of similar circuits on an integrated circuit (IC) or "chip" allows the overall size and cost of the circuit to be decreased, and also provides fewer interconnections, increasing reliability.

Accordingly, it would have been readily obvious to one of ordinary skill in the art at the time the claimed invention was made to provide the plurality of EEPROM memory circuits in Sukegawa et al (U.S. '001) "in a chip," and to control the activity and inactivity of each of the memory circuits "by inputting a command," as taught by Lee et al, in order to selectively allow

certain memory arrays or circuits on the chip to be made "active" or "inactive" for read and write operations, and to obtain smaller overall size and cost and improved reliability, all highly desirable features in a semiconductor memory such as in Sukegawa et al (U.S. '001).

Since applicant's claims "read on" a structure and method rendered obvious to one of ordinary skill in the art by the combined teachings of the references, the invention as set forth in the claims would have been obvious, within the meaning of 35 U.S.C. 103, in light of the prior art.

With respect to claim 6, a common chip enable terminal may be provided for the plurality of memory circuits in Lee et al since the activity and inactivity of the memory circuits may be selected by inputting a command, so that a common enable signal inputted to the chip enable terminal is supplied to a selected one of the memory circuits which has been selected by inputting the command, in order to provide a simply selection mechanism for the plurality of memory circuits which are provided on the same chip, as taught by Lee et al.

With respect to claim 7, two of the memory circuits in Sukegawa et al (U.S. '001) and Lee et al may be alternatively enabled so as to interleave operations in a well known manner.

11. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sukegawa et al (U.S.'001) and Lee et al, taken together, as applied to claims 5-7 above, and further in view of Bruce et al.

Sukegawa et al ('001) in view of Lee et al discloses an electrically rewritable nonvolatile semiconductor memory device, such as an electrically erasable programmable read only memory

(EEPROM), including a plurality of "memory circuits," each having a ready/busy terminal as in the claimed invention (see numbered paragraphs 8 and 9 above, e.g.), but does not teach providing a common ready/busy signal terminal for the plurality of memory circuits, with the ready/busy state of a selected one of the memory circuits being output to a ready/busy signal terminal.

Bruce et al similarly discloses an electrically rewritable nonvolatile semiconductor memory device including a plurality of memory circuits, each having a ready/busy terminal, and also teaches providing a common ready/busy signal terminal for the plurality of memory circuits, with the ready/busy state of a selected one of the memory circuits being outputted to a ready/busy signal terminal. In this manner, the ready/busy state of all memory circuits in a "bank" or group may be easily monitored without polling the status of each of the memory circuits [see column 3, lines 19-32; column 9, lines 6-12; column 13, lines 20-21; and Figures 4 and 5, e.g.].

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to provide a common ready/busy signal terminal for a plurality of memory circuits, with the ready/busy state of a selected one of the memory circuits outputted to a ready/busy signal terminal, as taught by Bruce et al, in the nonvolatile memory including a plurality of memory circuits such as in Sukegawa et al (U.S. '001) and Lee et al, taken together, as previously discussed, in order to quickly and easily monitor the ready/busy states of the memory circuits.

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Watanabe is cited as disclosing an electrically rewritable nonvolatile semiconductor memory device including a plurality of memory circuits or blocks provided in a memory chip, wherein the "activity" and "inactivity" of each of the plurality of memory circuits is controlled by an enable signal or terminal similar to the present invention.

Kaki et al is cited as disclosing an electrically rewritable nonvolatile semiconductor memory device including a plurality of memory circuits in which instructions may be sequentially sent to different flash memories to continuously write data in the plurality of memories via a data buffer, similar to the present invention.

Kikuchi et al is cited as disclosing an electrically rewritable nonvolatile semiconductor memory device including a plurality of memory circuits, wherein the activity and inactivity of each of the plurality of memory circuits is controlled by a chip enable terminal, similar to the present invention.

Sukegawa (U.S. '814) is cited as disclosing an electrically rewritable nonvolatile semiconductor memory device including a plurality of memory circuits, wherein the activity and inactivity of each of the plurality of memory circuits is controlled by a chip enable terminal and each of the plurality of memory circuits includes a ready/busy terminal similar to the present invention.

Satoshi is cited as disclosing an electrically rewritable nonvolatile semiconductor memory device including a plurality of memory circuits in which data may be continuously written, the memory circuits being coupled to a shared data bus and having respective chip enable terminals to control the activity and inactivity of the memory circuits, similar to the present invention.

Shinji is cited as disclosing an electrically rewritable nonvolatile semiconductor memory device including a plurality of memory circuits, each having a chip enable terminal, wherein the activity and inactivity of each of the plurality of memory circuits is controlled by chip enable signals which are controlled based on decoding results.

Toru et al is cited as disclosing an electrically rewritable nonvolatile semiconductor memory device including a plurality of memory circuits, each having a chip enable terminal, wherein writing operations to successive addresses in the plurality of memory circuits may be quickly performed similar to the present invention.

It is also noted here that the Information Disclosure Statement (IDS) filed September 6, 2002 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 and has NOT been considered because a translation of the relevant portions of the non-English language reference was not provided. The IDS has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of

determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609 C(1).

[Note that while an English language abstract may sometimes satisfy the statement of relevance requirement for a non-English language publication, it is not sufficient here since the reference was cited in a Korean Office action (see page 1 of the IDS) and the abstract does not sufficiently explain the reference's relevance or why it was cited in the Korean Office action. A translation of the relevant portions of the Korean Office action should also be provided for proper consideration by the Examiner.]

It is also noted here that due to the number and nature of the 35 U.S.C. 112, second paragraph, issues outlined above, no prior art is being applied against claims 11-14, and the subject matter therein not indicated as allowable, since the Examiner cannot ascertain, with a reasonable degree of certainty, the intended meaning and scope of the claims. In this regard, see In re Steele, 305 F.2d 859, 134 USPQ 292 (CCPA 1962). In this regard, also see MPEP 2173.03 and 2173.06, as well as the comments in numbered paragraph 7 above.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn Gossage whose telephone number is (703) 305-3820.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Do Yoo, can be reached on (703) 308-4908.

The fax phone numbers for the organization where this application or proceeding is assigned are as follows:

(703) 746-7238	(After Final Communications)
(703) 746-7239	(Official Communications)

(703) 746-5713 (Use this FAX number only after approval by the Examiner, for "INFORMAL" or "DRAFT" communications. An Examiner may request that a formal paper/amendment be faxed directly to him or her on occasion.)

GLENN GOSSAGE
PRIMARY EXAMINER
ART UNIT 2187